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Photonic Silicon Device Physics

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This research program investigated the fundamental mechanisms involved in light-emitting silicon structures, fabricated silicon-based photonic devices, and examined the electrical device properties. The approach evolved into the study of three distinct areas of interest: porous silicon layers, silicon microplasmas, and silicon nanostructures. These three areas are related by the need for understanding materials properties on the nanometer size scale and the need for applying microelectronic-device-fabrication techniques to aid in elucidating the emission mechanisms and to ultimately transition such knowledge into practical electronic devices. The document summarizes the work completed to date in each of these areas.

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This program investigated the fundamental mechanisms involved in light-emitting silicon structures, fabricated silicon-based photonic devices, and examined the electrical device properties. The approach evolved into the study of three distinct areas of interest: porous silicon layers, silicon microplasmas, and silicon nanostructures. These three areas are related by the need for understanding materials properties on the nanometer size scale and the need for applying microelectronic-device-fabrication techniques to aid in elucidating the emission mechanisms and to ultimately transition such knowledge into practical electronic devices. The following paragraphs summarize the work completed to date in each of these areas.

BACKGROUND AND OBJECTIVE

Silicon, because of its process maturity, low cost, high yield, and reliability, is the material of choice for large levels of electronic device integration. Recent research and development of novel silicon-based technologies (e.g., silicon-germanium alloys, silicon on insulator (SOI), silicon on sapphire (SOS)) have resulted in high-speed performance approaching that offered by group III–V and II–VI semiconductors. The remaining limitation of silicon for optoelectronic applications is the indirect band gap, which has, heretofore, prevented direct optical transitions that could provide an efficient photonic (light-emitting) source compatible with silicon processing. The availability of a photonic silicon source would allow a breakthrough in optoelectronic integrated circuits with applications in optical computing, high-speed communications, and integrated sensor and smart sensor technology. Additional applications include light-emitting diodes (LEDs), flat-panel displays, and optical interconnections critical for advances in future generation Navy C^4I platforms and systems.

POROUS SILICON DEVICES

Since the discovery of photoluminescent porous silicon (Canham, 1990), porous silicon has emerged as a potential photonic source compatible with silicon microelectronics. The light emission mechanism, however, is still not fully understood. The predominant theory is related to the confinement of electrons and holes in a silicon wire or particle with dimensions on the order of tens of nanometers. In such cases, it is hypothesized that the electrons and holes may recombine and efficiently emit light if there are few nonradiative mechanisms competing for the charge carriers. This theory, called quantum confinement, has been observed in other materials systems and has been theoretically modeled in silicon (Ohno et al., 1992; Sawada et al., 1994). These silicon nanoparticles or nanowires are predicted to have a direct band gap, thus allowing efficient electron-hole recombination without employing the less efficient phonon-assisted transitions. Other theories note that silicon compounds such as amorphous silicon, silicon oxides, and siloxene derivatives also luminesce in the visible region of the spectrum and propose those models as a source of the luminescence (Perez et al., 1992; Milewski et al., 1994; Brandt et al., 1992).

Typically, the method of fabricating porous silicon layers in bulk silicon wafers uses an anodic oxidation process with a backside contact to the silicon anode and a platinum (Pt)

counter-electrode in a hydrofluoric acid (HF) and ethanol solution (Canham, 1990; Bsiesy et al., 1991). By using low current densities, silicon wafers are made porous by the electrochemical dissolution of silicon, as schematically shown in figure 1. Figure 1(a) schematically shows a plan view of partially anodized (100)-oriented silicon with 25-percent porosity (i.e., the silicon has been removed from one-quarter of the volume). Figures 1(b) and 1(c) show the effect of increased etching, which enlarges the pores or voids until they subsequently intersect leaving a matrix of isolated wires. Porosity exceeding approximately 65 percent is required to observe photoluminescence. In reality, the electrochemical dissolution is not as uniform, and the result is a dendritic structure of silicon wires in a complex matrix. A scanning electron microscope (SEM) photomicrograph of the cross section of an anodically oxidixed porous silicon layer is shown in figure 2.

In this project, we explored novel thin films of porous silicon on transparent insulating substrates (sapphire and quartz), which allowed the elimination of interactions with and contribution from the bulk by etching the entire silicon layer. This aided in the elucidation of the photoluminescence mechanism by independently allowing the examination of the porous layer. In addition, the transparent substrates allowed for unique analysis of the optical properties from either side of the porous layer and allowed the design of photonic devices using conventional (opaque) metals.[1,2] Due to the insulating nature of the transparent substrates, the studies described here typically use a stain etch composed of HF, nitric acid (HNO_3), and distilled water in a ratio of 1:5:10 (Fathauer et al., 1992; Sarathy et al., 1992) to form the porous layers without need for electrical contact to the backside of the wafer. An alternative technique was developed in this program by using optical excitation rather than electrical contact to form porous silicon. Details have been published in Dubbelday et al. (*MRS Proc*., 1993a) and Dubbelday et al. (1993b). Figure 3 shows a cross-sectional SEM photomicrograph of ~10 micron thick porous silicon layer on a sapphire (Al_2O_3) substrate fabricated using the purely chemical or stain-etching process. Figure 4 shows the photoluminescence spectra of a porous SOS film. The porous SOS sample shows photoluminescence signals comparable to those published for porous bulk silicon. The two curves shown are the emission spectra obtained when the sample is illuminated and emission collected at the silicon side (dotted line) and at the sapphire side (solid line) of the wafer. The photoluminescence maximizes in intensity at ~700 nm with a width of ~100 nm. The luminescence from the Cr^{+3} impurity (695 nm) is pronounced in the sapphire-side emission spectrum. This peak occurs since the sapphire substrate used in this case was from a Czochralski (CZ) grown boule that had trace impurities from the growth of ruby laser crystals (chromium-doped sapphire). This peak does not occur in edge-fed-growth (EFG) sapphire available from other manufacturers. The similarity in the front and backside porous silicon spectra suggests uniformity in the porous structure with depth, and that strain effects due to the lattice mismatch between the silicon and the sapphire are minimal. Photoluminescent films were obtained in porous films ranging in thickness from 10 microns to as thin as 90 nm (NRaD's ultrathin SOS, see Offord, 1992). Further analyses of the morphological differences and strain effects of porous SOS structures have been published (Dubbelday et al., 1993b).

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[1]Russell, S. D., W. B. Dubbelday, R. L. Shimabukuro, P. R. de la Houssaye, and D. M. Szaflarski, "Photonic Silicon on a Transparent Substrate," Navy case 75,292, filed 9 September 1993; patent pending.

[2]Dubbelday, W. B., R. L. Shimabukuro, and S. D. Russell, "Electroluminescent Devices in Porous Silicon on Sapphire," Navy case 76,291, disclosure submitted 26 January 1993.

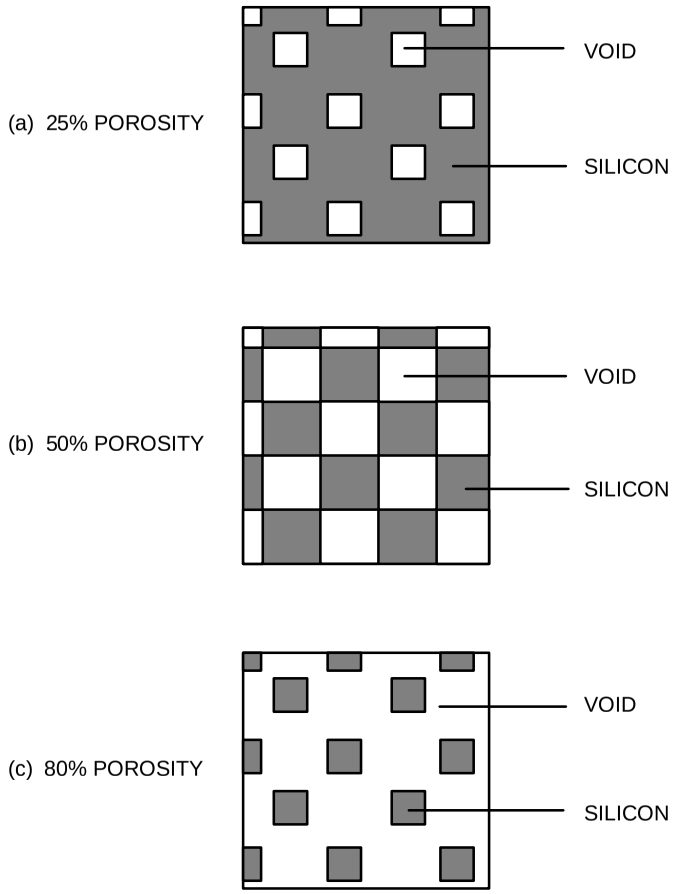

Figure 1. Schematic plan view of porous silicon.

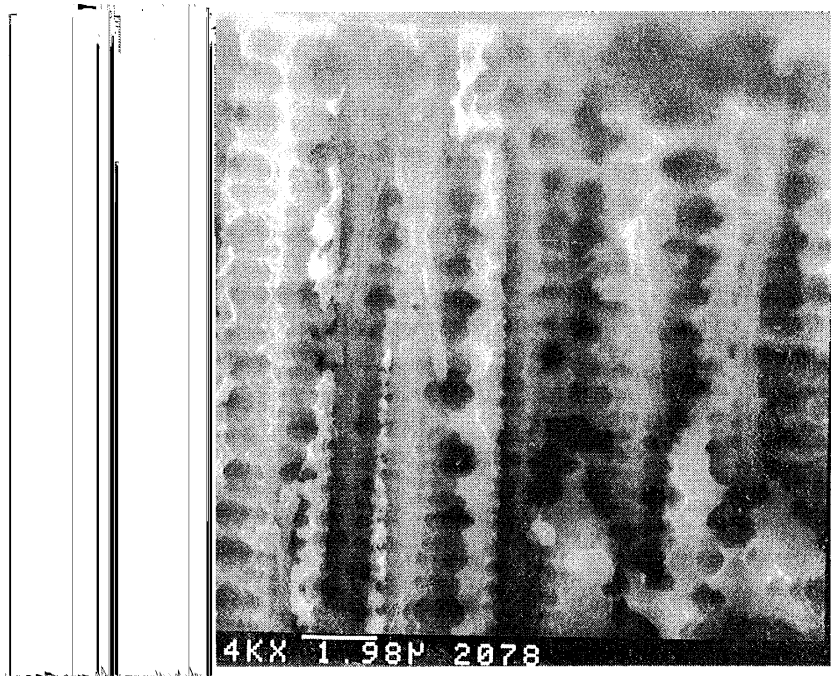

Figure 2. SEM cross section of porous silicon.

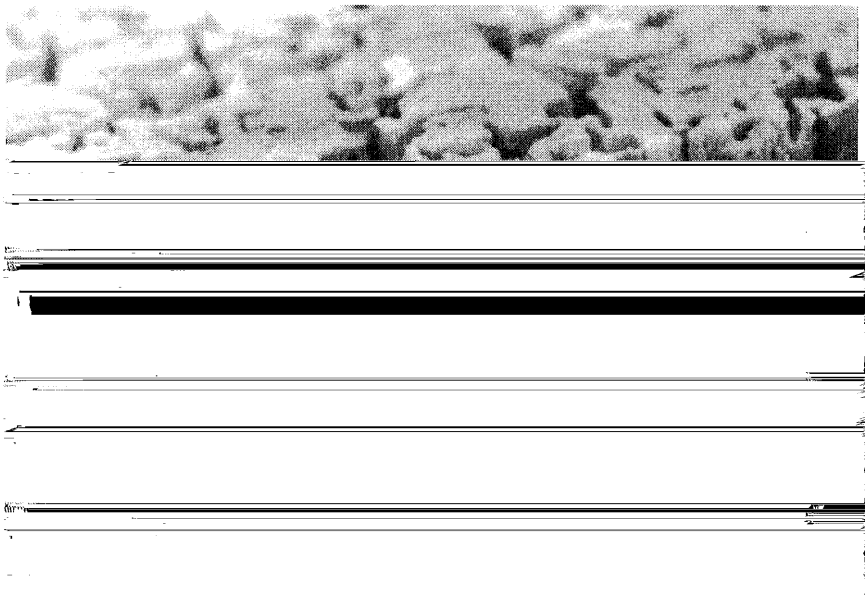

Figure 3. SEM cross section of porous SOS.

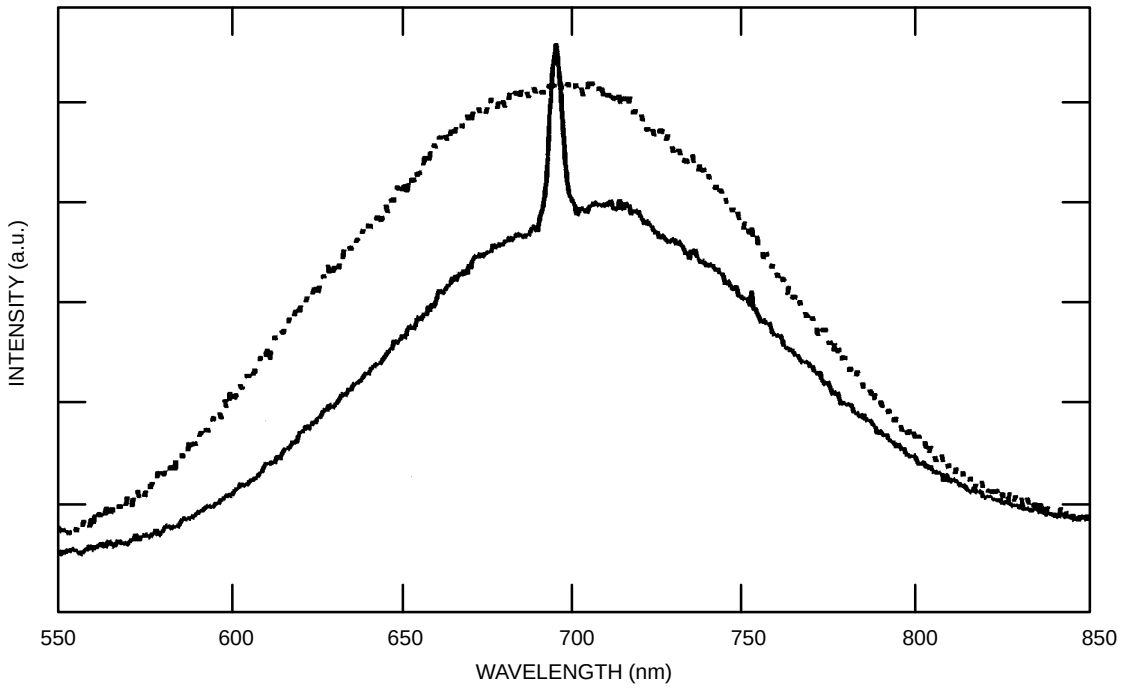

Figure 4. Photoluminescence spectra of porous SOS.

An investigation into the dependence of porous silicon photoluminescence on the crystallinity of the starting silicon layers was completed to elucidate the light emission mechanism by decoupling the surface species formed by the chemistry from the crystalline state of the nanostructures. This study applied identical etch procedures to crystalline, damaged, and amorphous silicon layers to examine the emission mechanism. Ion implantation was employed to control the degree of crystalline damage prior to the fabrication of the porous layer. The data indicated that crystalline order is required for photoluminescent porous silicon. The lack of photoluminenescence from an amorphous silicon layer etched identically to bulk silicon is consistent with the absence of photoluminescence from porous silicon layers fabricated in heavily ion-damaged amorphous silicon. These results are inconsistent with an amorphous silicon or siloxene emission mechanism, and suggest quantum confinement plays a role in the light emission of the porous silicon (Dubbelday et al., 1993a). The effects of etchant composition and microstructure on the photoluminescence of porous silicon has also been reported (Dubbelday et al., 1995). An alternative etchant using HF-sodium nitrite ($NaNO_2$) was developed with freely available NO_2 ions, which reduced the accelerated etching effects from ion implantation damage. Transmission electron microscopy (TEM) analysis of the porous silicon layer (figure 5a) shows lattice images of the crystalline portions. Figure 5b shows the electron diffraction pattern obtained, characteristic of a crystalline porous region.

SOS was fabricated in the as-deposited, improved (Garcia & Reedy, 1986), and bonded wafer forms. Each of the fabrication techniques imparts characteristic microcrystalline defects in the silicon layer. Microstructural defects such as microtwins and threading dislocations in the starting material had no observed effect on the light-emitting properties of porous SOS. Vacancies imparted by ion implantation damage, however, can amorphize the material resulting in a quenching of the photoluminescence. An apparent increase in the density of light-emitting structures leading to enhanced photoluminescence can also be obtained by limited ion damage of the material prior to the fabrication of the porous layer (Russell et al., 1994a). This may be employed to enhance light emission from porous silicon devices.[3]

Porous silicon LEDs have been reported using transparent (indium tin oxide known as ITO) and semitransparent (gold) electrodes (Koshida & Koyama, 1992; Namavar et al., 1992; Steiner et al., 1993). The electroluminescence spectra are similar to that of the photoluminescence spectra (i.e., peaked in the visible with broadband emission). Avoiding the use of nonstandard metals, such as ITO and gold, is a major manufacturing advantage offered by the transparent substrates studied in this project. Evaluation of microfabrication processes and their effect on the light emission of porous silicon was also performed. Thermal processing above about 300°

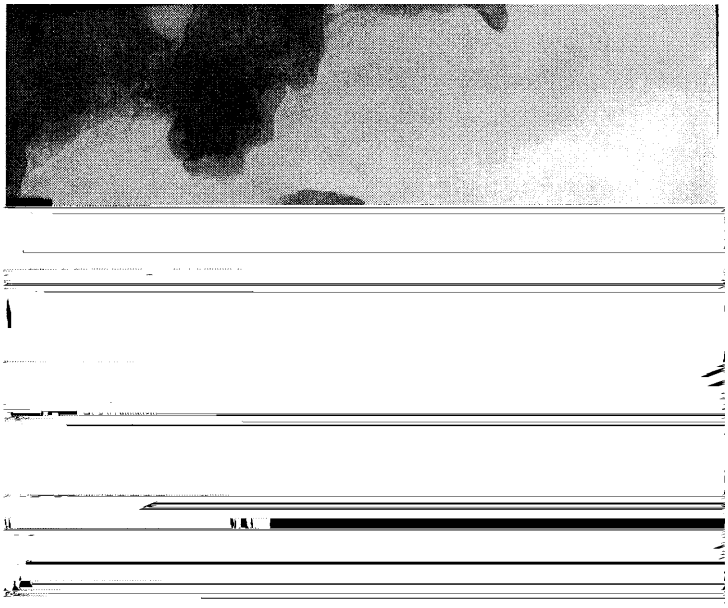

Figure 5a. TEM lattice images of porous silicon.

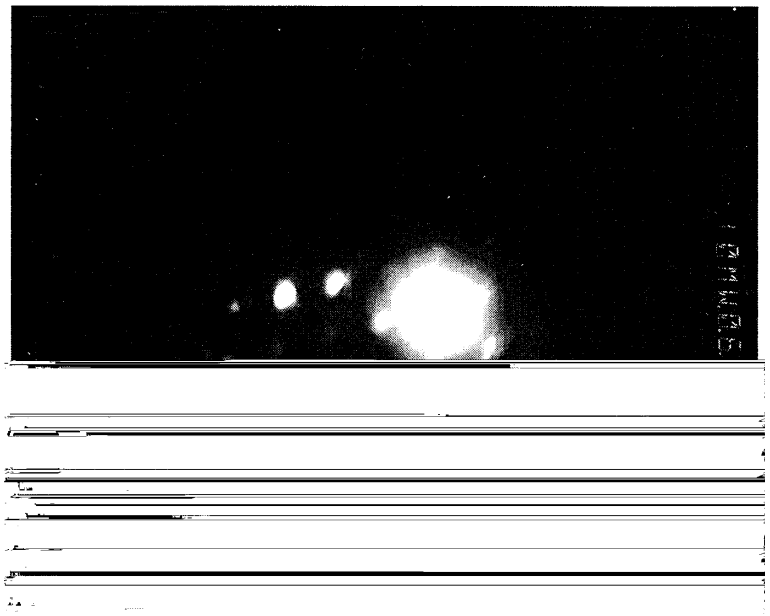

Figure 5b. Electron diffraction pattern of porous silicon.

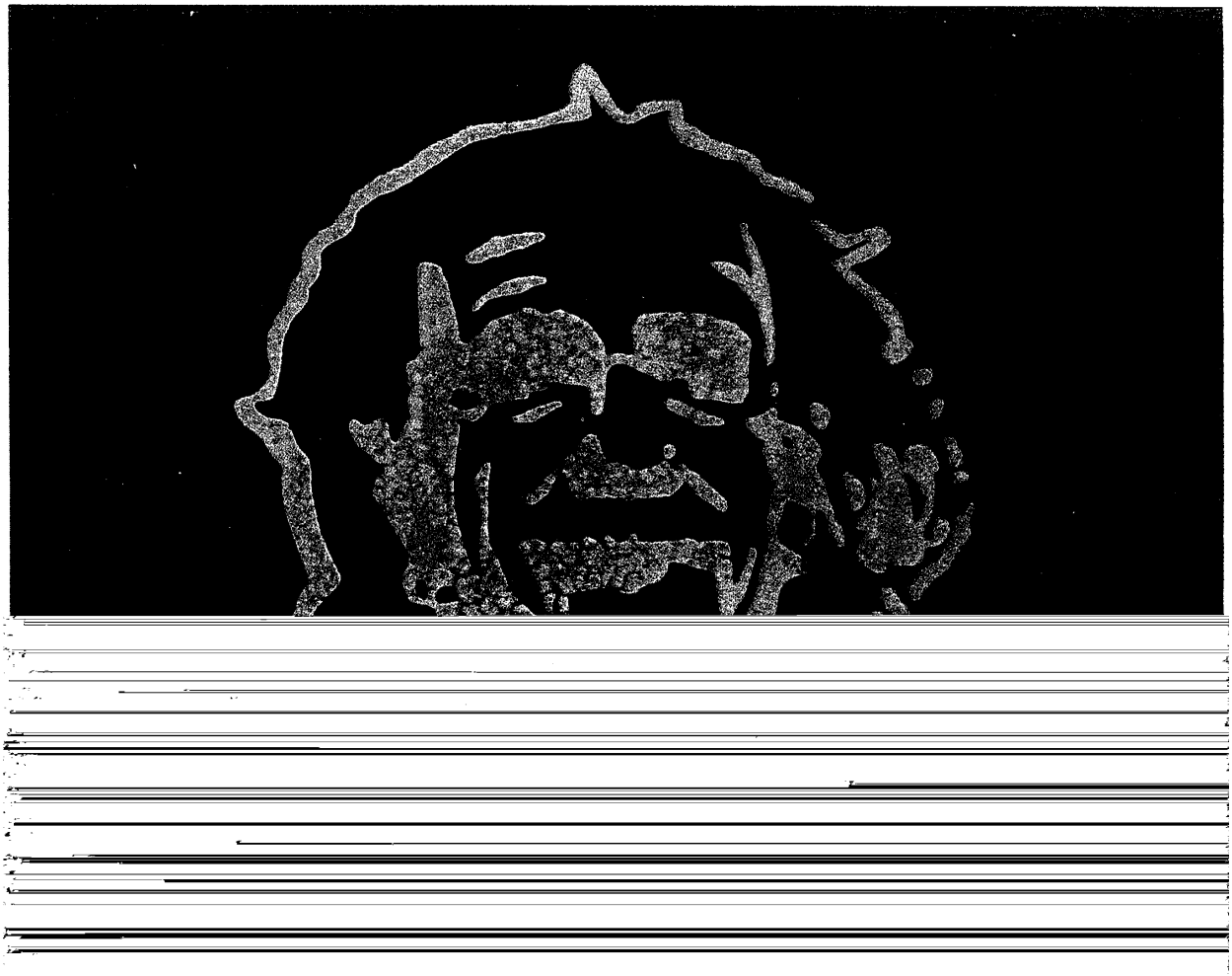

Figure 6. Photolithographically patterned porous silicon.

porous silicon and porous SOS and porous silicon on quartz (SOQ) was performed, in part, to replicate previous reports. Despite having good electrical resistivity and rectifying I-V behavior, no measurable electroluminescence has been observed on our devices to date. Photoluminescence of the underlying porous layer was still evident after ITO deposition suggesting that the porous nanostructures were undamaged by the processing and that improvement in charge injection efficiency is required in our porous silicon device design. Unlike a variety of solvents, use of aluminum to make electrical contact to porous silicon layers does not quench the photoluminescence (Russell, 1994b). Initial tests, however, have not demonstrated electroluminescence from simple device structures using aluminum. Figure 7 shows one design for a porous silicon LED currently in the early stages of fabrication. Variation in the device geometry (both lateral and vertical junction designs) have been employed in the newly designed photolithographic mask set, which will allow further examination of these devices.

SILICON MICROPLASMA DEVICES

Light emission from avalanche breakdown of silicon p-n junctions has been known since the early days of semiconductor research (Newman et al., 1955; Chynoweth & McKay, 1956; Rose, 1957; Davies & Storm, 1961). The light emitted from reverse-biased diodes is attributed to a phonon-assisted recombination of hot (high energy) electrons and holes in the region where avalanche breakdown is initiated. These avalanche regions have a high concentration of hot charge carriers that are produced by ionization of the silicon in large applied electric fields and are referred to as microplasmas. The characteristic emission spectra, while exhibiting high-energy visible photons (as high as ~3 eV), peak near the silicon bandgap at 1.1 eV in the infrared. An alternative interpretation of the emission mechanism (Figielski & Torun, 1962) is that of bremsstrahlung of hot carriers, rather than recombination, in the microplasma regions.

Microplasma emission is unlike the reported light emission from SOS diodes reverse biased into second (thermal) breakdown (Dumin, 1969). In such cases, the diode exhibits a current-controlled negative resistance region in the I–V characteristics with the formation of a filament of high local current density. This effect occurs after the onset of the weaker emitting silicon microplasmas. While light emitted from diodes in the second breakdown does not have the spectra characteristic of an incandescence, the emitted intensity increases in the infrared region near 1.1 eV, similarly to those reported for the microplasmas. Most importantly, these effects occur prior to the onset of incandescence, and are not simply blackbody emission from a thermal body.

In this program, we have fabricated microplasma devices in the ultrathin layers of SOS described previously. The devices employ a simple p-n rectifying junction through which charge injection occurs. Conventional opaque metal (aluminum) is used for electrical contact; therefore, light emitted from these devices is detected through the transparent sapphire substrate. Forward-biased ultrathin SOS devices do not emit light, whereas reverse-biased devices emit broadband light. The onset of light emission occurs at voltages as low as 4 volts. Characteristic I–V curves, shown in figure 8, do not show the negative resistance regions observed in second (thermal) breakdown. Signatures of microplasma behavior, however, do exist, in addition to the reverse biasing required for light emission. Figures 9(a) and (b) show optical photographs of the emitted light along a junction of the SOS microplasma LED. The observed distribution of discrete microplasmas along the junction is typical of the previously reported microplasmas. Increase in

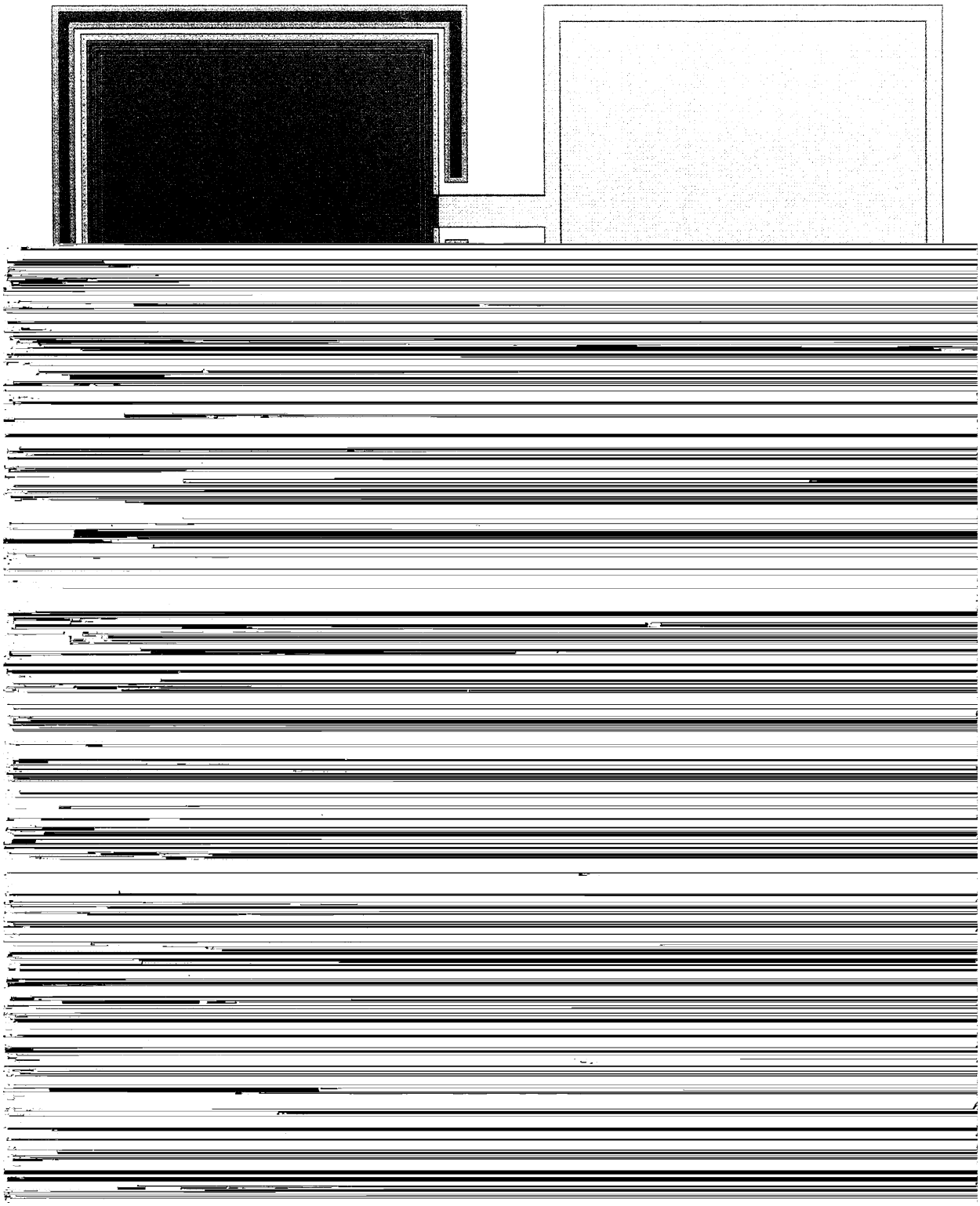

Figure 7. Porous SOS LED design.

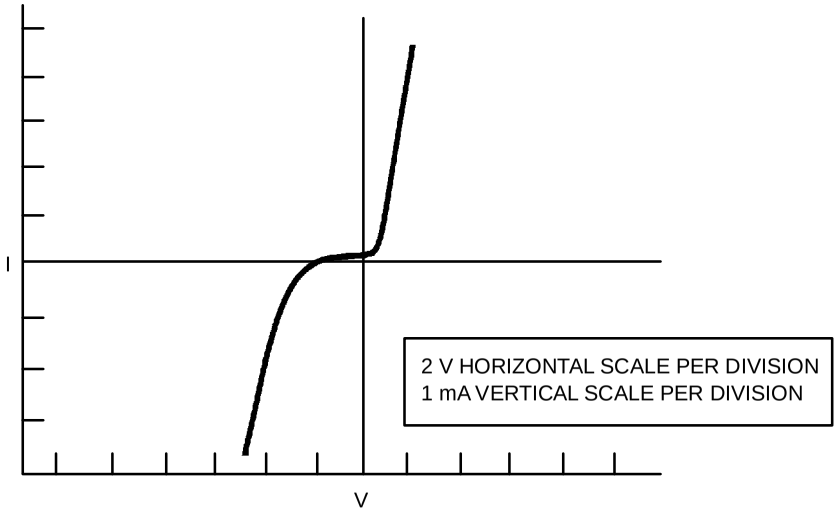

Figure 8. Microplasma LED I-V characteristics.

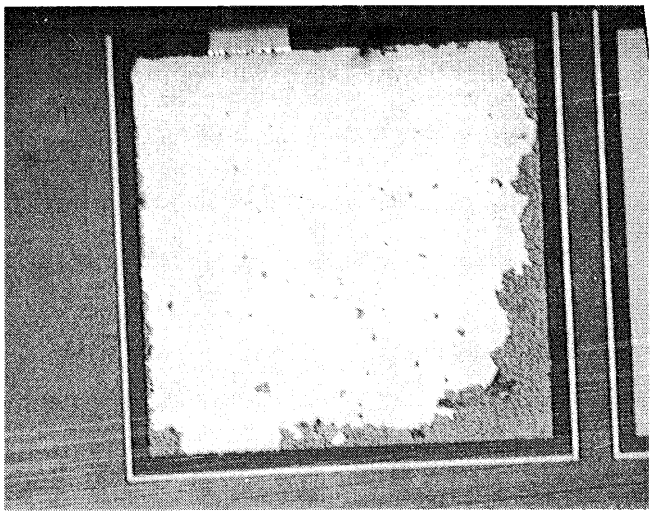

Figure 9a. Light emission from SOS microplasma LED.

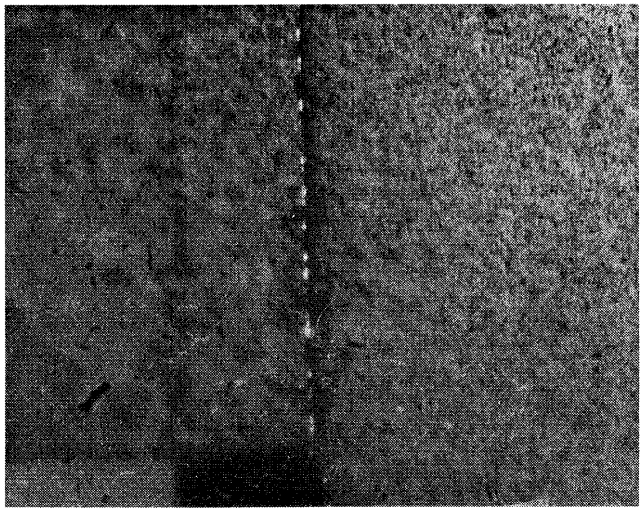

Figure 9b. Closeup view of microplasma emission.

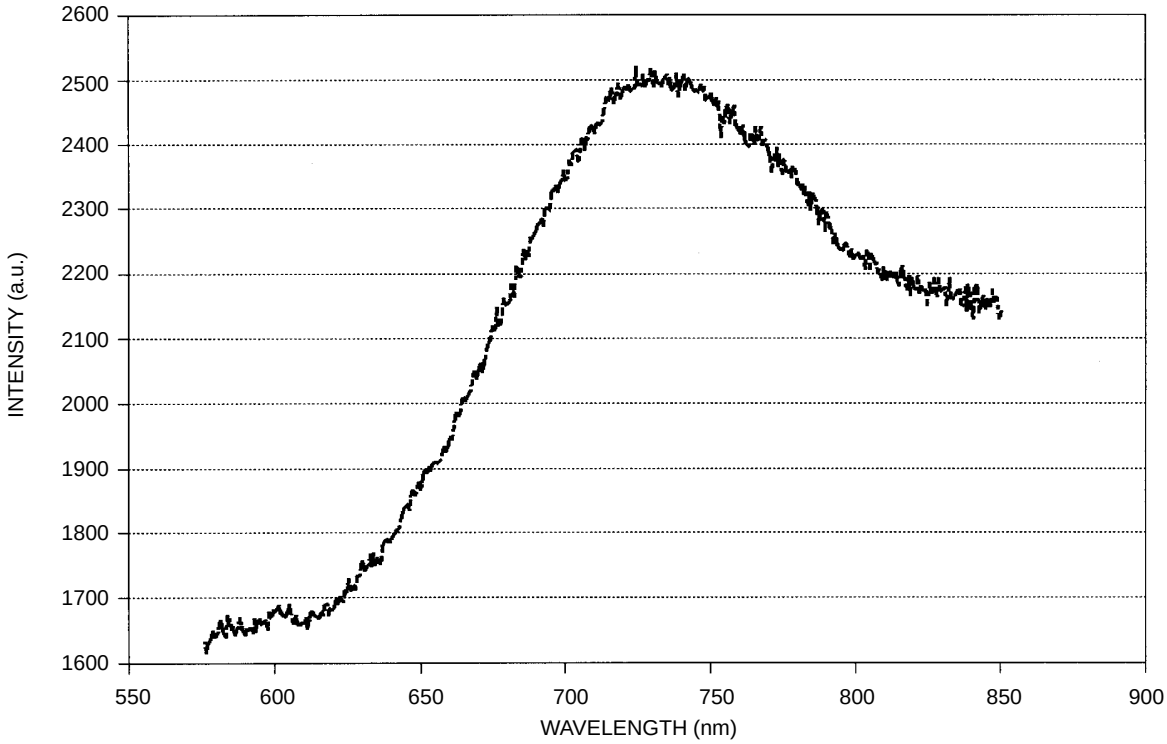

Figure 10. SOS microplasma LED emission spectrum.

reverse-bias voltage (and corresponding increase in drive current) produces an increase in light emission, corresponding to an increase in the number of microplasmas. However, we have discovered new features that differ from earlier reports. The emission spectrum from the reverse-biased SOS microplasma LED are shown in figure 10 (corrected for spectrometer response). The peak of the light emission is in the visible region, unlike that previously reported for diodes in avalanche or thermal breakdown. In addition, a temperature dependence in opposition to prior reports (Kosyachenko et al., 1990; Lanzoni et al., 1991) of silicon hot-carrier light emission is observed. The integrated intensity (between 550 and 850 nm) at room temperature (296 K) is greater than four times that of the device at liquid nitrogen (77 K) temperature. When the device is heated to 398 K, the integrated intensity further increases to greater than 15 times the emission at cryogenic temperatures. The peak intensity also follows similar behavior. These deviations from previously reported microplasmas are, at this time, attributed to the highly stressed ultrathin silicon film and the reduced carrier lifetime in the ultrathin SOS. Since the charge carrier lifetime is substantially shorter in SOS compared to bulk silicon due to defect scattering, the increased electron-phonon scattering will affect the ionization rate (Wolff, 1954). Raman spectroscopic measurement of stress in ultrathin SOS films (Dubbelday et al., 1993a, b) shows that the silicon layer is under a large compressive stress ($\sim 5 \times 10^9$ dynes/cm^2). Such stresses are sufficient to modify the electronic band structure, which has been demonstrated with increased hole mobility and decreased electron mobility compared to bulk silicon (Garcia & Reedy, 1986). This intrinsic stress, caused by the thermal expansion mismatch between the silicon and the underlying sapphire, may be sufficient to shift the peak of the emission spectrum of the hot carriers into the visible region. Further experiments are in progress to fully identify these anomalous microplasma results. Figure 11 shows one design for an ultrathin SOS microplasma LED currently in the early stages of fabrication. Variations in junction and device geometry have been employed in the newly designed photolithographic mask set which will aid in the elucidation of these questions.

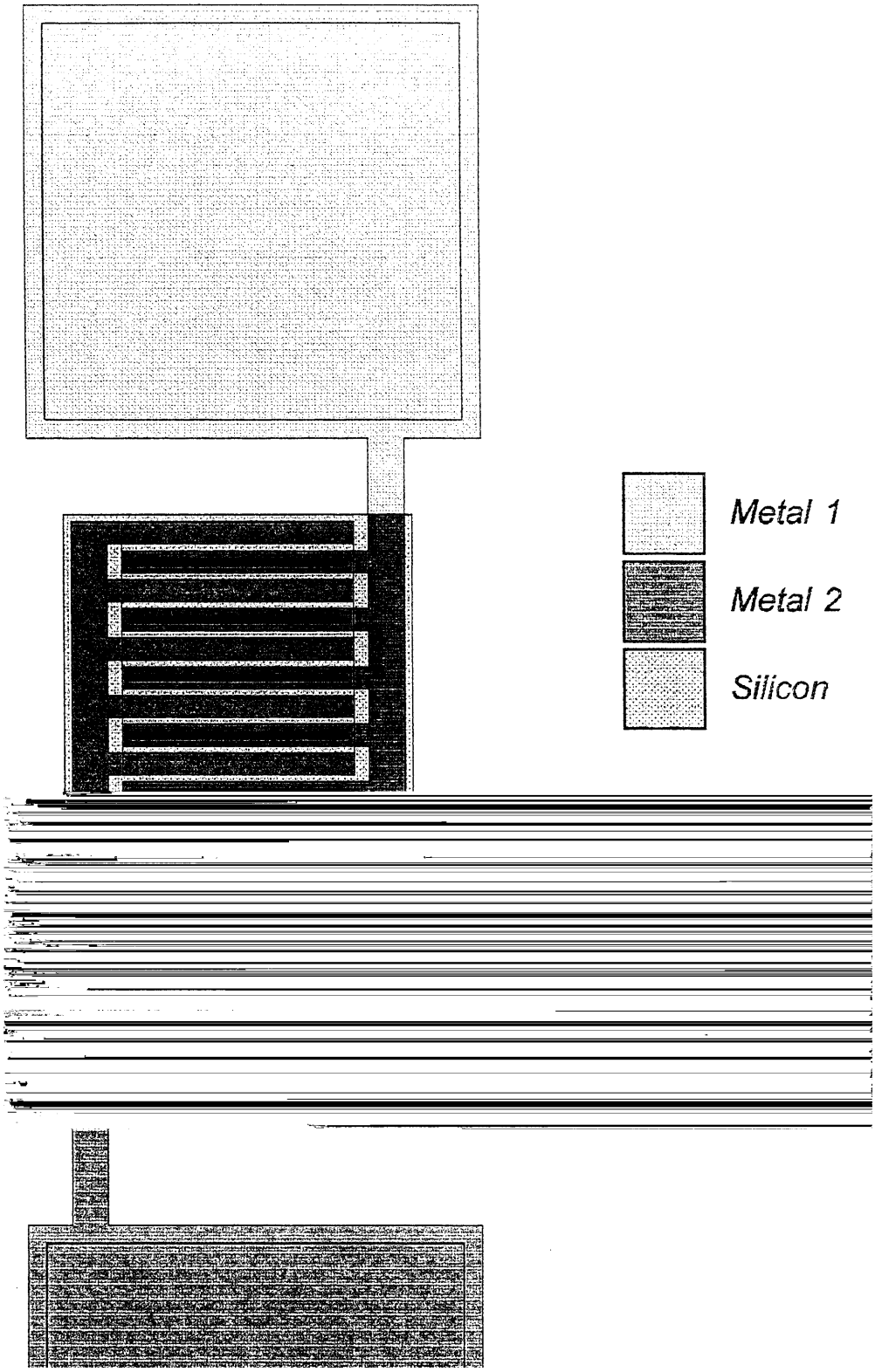

Figure 11. Ultrathin SOS microplasma LED design.

SILICON NANOSTRUCTURED DEVICES

As requirements for increased speed and performance push silicon fabrication methods to smaller dimensions, nanofabrication techniques and quantum effects in semiconductors become important technological issues. The recent developments in photoluminescent porous silicon and porous SOS discussed above have hinted that possible quantum confinement effects may alter the 1.1-eV indirect bandgap structure in silicon to allow for the efficient emission of visible light as described above. Fabrication of vertical nanowires in an attempt to directly test this theory has been reported in bulk silicon crystals (Lui et al., 1993). One of the disadvantages of this technique results from the nonuniformity of the thinning oxidation, which produces a structure of varying width.

In this work, NRaD, in collaboration with the Physics, Chemistry, and Electrical Engineering Departments at the University of California, San Diego; the Department of Materials Science and Materials Engineering at the University of California, Berkeley; and Digital Instruments, harnessed the unique properties of a high-quality single crystal film of silicon on sapphire and used the film thickness as one of the confinement dimensions. Lateral arrays of silicon nanowires were fabricated in the thin (5- to 20-nm) silicon layer and studied (Dubbelday et al., 1994). This technique offers simplified contact to individual wires and provides wire surfaces that are more readily accessible for controlled alteration and device designs.[5] (100)-oriented silicon was deposited by chemical vapor deposition (CVD) on crystalline sapphire and crystal quality was improved using solid-phase epitaxy techniques (Garcia & Reedy, 1986). The silicon layer was subsequently thinned by oxidation and etching of the oxide layer. The thinned silicon layer on sapphire chips was coated with an electron-beam-sensitive photoresist, and individual lines 50 nm wide and 20 microns long were written in an array using a JEOL JSM–6400 electron-beam lithography system, which provided a 3-nm spot size. After resist development, the pattern was reactively ion-etched into the thin silicon using an oxygen-dichlorodifluoromethane (CCl_2F_2) plasma to form the lateral nanowires. The resist was removed prior to examination. An alternative technique using monolayer etching of the silicon using an oxide mask and single layers of adsorbed chlorine was also tried to eliminate potential reactive ion-etch damage. This technique was extremely selective, i.e., there was little reaction with the SiO_2, so that undesired oxide-micromasked regions prevented uniform etching, which resulted in severe surface roughening.

The initial reactive ion-etched patterns were observed using scanning electron microscopy, and the larger arrays could be seen through an optical microscope (figure 12). Individual wire details were examined using atomic force microscopy (AFM). Figure 13 shows an AFM analysis of a single silicon nanowire with dimensions of less than 18 nm in height and approximately 100 nm across. To date, no visible photoluminescence has been observed from these lateral nanostructures. Controlled oxidation studies for thinning these 100-nm wires down to sub-10-nanometer sizes are underway. Subsequent examination of the light-emitting properties from individual nanowires will be performed using near-field microscopic techniques (Diaspro, 1994).

[5]S. D. Russell, R. C. Dynes, P. R. de la Houssaye, W. B. Dubbelday, A. S. Katz, and R. L. Shimabukuro, "Silicon Nanostructures in Silicon on Insulator," Navy case 76,969, disclosure submitted 22 November 1994.

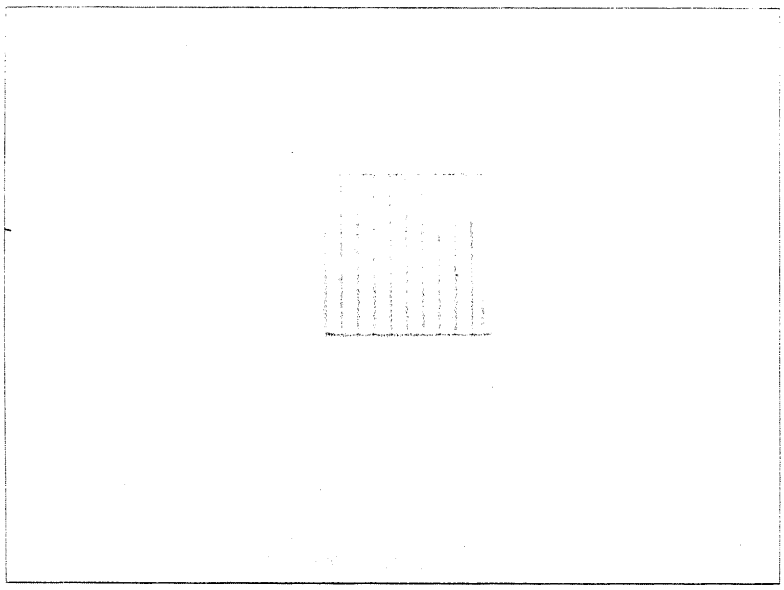

Figure 12. Optical micrograph (1000X) of nanowire array.

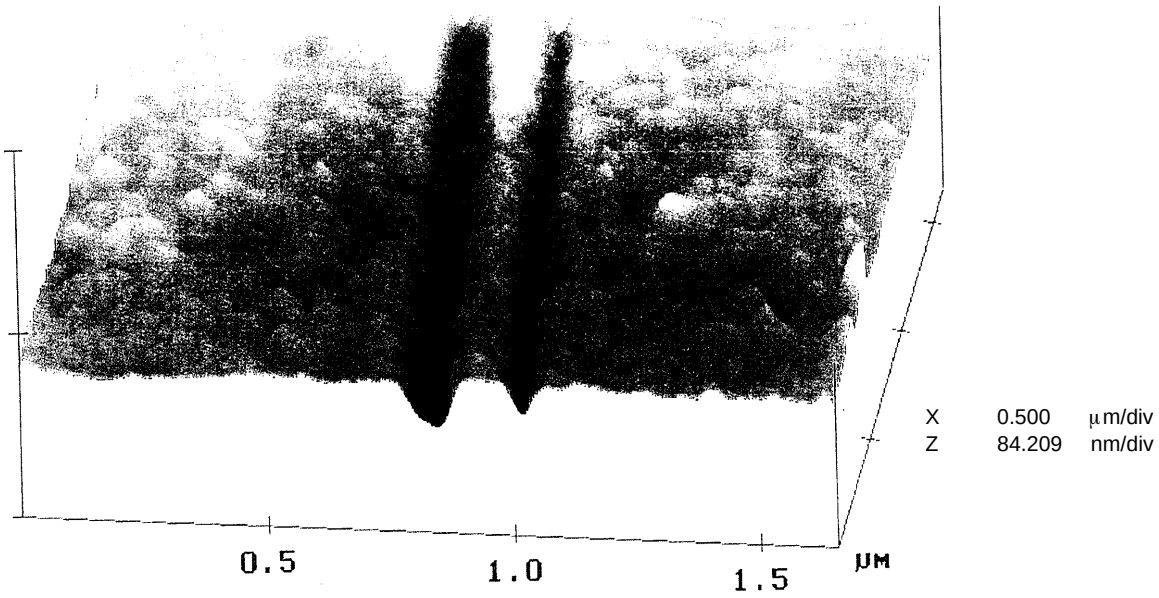

Figure 13. AFM profile of one nanowire.

SUMMARY AND NAVY SIGNIFICANCE

A variety of novel silicon devices have been fabricated and their light-emitting properties studied during this project. Porous silicon, porous SOS, and porous SOQ exhibit strong photoluminescence with quantum efficiencies as large as 10 percent; however, this project has yet to demonstrate electroluminescence due, in part, to difficulties in making efficient electrical contact to the porous structures. We hope that modified device designs, currently in fabrication, will overcome this limitation. Lateral silicon nanowires on sapphire have been fabricated, and future tests will be performed on the validity of the quantum confinement theory in this materials system. Long-lived SOS microplasma LEDs have been fabricated that exhibit visible light emission at low voltages. Improvements in device design have been completed, and further study of the anomalous emission spectrum will be finished following completion of the current wafer lot.

These preliminary results have generated interest from several Navy sources. The Office of Naval Research (ONR) Solid State Materials program supported preliminary research on porous silicon device processing for potential solid-state, laser-pumping applications (Russell et al., 1993). ONR's Microelectronics program is interested in the technology for use in advance optical interconnection systems. The Strategic Systems Program Office is currently evaluating the technology as a chemical sensor for use in real-time environmental diagnostics and reliability tests and enhancements to guidance systems.[6,7]

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REFERENCES

Brandt, M. S., H. D. Fuchs, M. Stutzmann, J. Weber, and M. Cardona. 1992. "The Origin of Visible Luminescence from 'Porous Silicon': A New Interpretation," *Solid State Communications*, vol. 81, no. 4, pp. 307–312.

Bsiesy, A., J. C. Vial, F. Gaspard, R. Herino, M. Ligeon, F. Muller, R. Romestain, A. Wasiela, A. Halimaoui, and G. Bomchil. 1991. "Photoluminescence of High Porosity and of Electrochemically Oxidized Porous Silicon Layers," *Surface Science*, vol. 254, pp. 195–200.

[6]S. D. Russell, "Energy Converting Porous Silicon Optical Element," Navy case 76,947, disclosure submitted 19 October 1994.
[7]S. D. Russell and W. B. Dubbelday, "Liquid Level Sensor and Detector," NCCOSC case 183.

Canham, L. T. 1990. “Silicon Quantum Wire Array Fabrication by Electrochemical and Chemical Dissolution of Wafers,” *Applied Physics Letters*, vol. 57, no. 10, September, pp. 1096–1098.

Chynoweth, A. G., and K. G. McKay. 1956. “Photon Emission from Avalanche Breakdown in Silicon,” *Physical Review*, vol. 102, no. 2, April, pp. 369–376.

Davies, L. W., and A. R. Storm, Jr. 1961. “Recombination Radiation from Silicon under Strong-Field Conditions,” *Physical Review*, vol. 121, no. 2, January, pp. 371–387.

Diaspro, A. 1994. “Application of Near-Field Optical Interactions to Microscopy,” *USA Microscopy and Analysis*, July, pp. 21–24.

Dubbelday, W. B., S. D. Russell, A. S. Katz, M. Winton, M. A. Wendman, P. R. de la Houssaye, R. C. Dynes, K. L. Kavanagh, A. C. Kummel, R. L. Shimabukuro & R. Gronsky. 1994. “Fabrication of Single Crystal Silicon Nanowires on a Sapphire Substrate,” 27th Annual Symposium of the Southern California Chapter of the American Vacuum Society Abstracts, 13 September, p. 27.

Dubbelday, W. B., S. D. Russell, K. L. Kavanagh. 1995. “The Effect of Starting Silicon Crystal Structure on Photoluminescence Intensity of Porous Silicon,” *Materials Research Society Proceedings*, to be published.

Dubbelday, W. B., D. M. Szaflarski, R. L. Shimabukuro, and S. D. Russell. 1993a. “Study of Thin Film Porous Silicon on Sapphire,” *Materials Research Society Proceedings*, vol. 283, pp. 161–166.

Dubbelday, W. B., D. M. Szaflarski, R. L. Shimabukuro, S. D. Russell, and M. J. Sailor. 1993b. “Photoluminescent Thin Film Porous Silicon on Sapphire,” *Applied Physics Letters*, vol. 62, no. 14, April, pp. 1694–1696.

Dumin, D. J. 1969. “Emission of Visible Radiation from Extended Plasmas in Silicon Diodes During Second Breakdown,” *IEEE Transactions On Electron Devices*, vol. ED-16, no. 5, May, pp. 479–485.

Fathauer, R. W., T. George, A. Ksendzov, and R. P. Vasquez. 1992. “Visible Luminescence from Silicon Wafers Subjected to Stain Etches,” *Applied Physics Letters*, vol. 60, no. 8, pp. 995–997.

Fgielski, T., and A. Torun. 1962. “On the Origin of Light Emitted from Reverse Biased p-n Junctions,” *Proceedings of the Sixth International Conference on Physics of Semiconductors*, London: Institute of Physics, pp. 863–868.

Garcia, G. A., and R. E. Reedy. 1986. “Electron Mobility Within 100 nm of the Si/Sapphire Interface in Double-Solid-Phase Epitaxially Regrown SOS,” *Electronics Letters*, vol. 22, no. 10, May, pp. 537–538.

Koshida, N., and H. Koyama. 1992. “Visible Electroluminescence from Porous Silicon,” *Applied Physics Letters*, vol. 60, no. 3, January, pp. 347–349.

Kosyachenko, L. A., E. F. Kukhto, V. N. Sklyarchuk, and V. A. Shemyakin. 1990. “Semiconductor Emitter Having the Spectrum of a Type A Source,” *Soviet Journal of Optical Technology,* vol. 57, no. 6, June, pp. 385–386.

Lanzoni, M., E. Sangiorgi, C. Fiegna, M. Manfredi, and B. Ricco. 1991. “Extended (1.1-2.9 eV) Hot-Carrier-Induced Photon Emission in n-Channel Si MOSFETs,” *IEEE Electron Device Letters*, vol. 12, no. 6, June, pp. 341–343.

Lui, H. I., P. K. Biegelsen, N. M. Johnson, F. A. Ponce, R. F. W. Pease. 1993. “Self-Limiting Oxidation of Si Nanowires,” *Journal of Vacuum Science and Technology B*, vol. 11, no. 6, pp. 2532–2537.

Milewski, P. D., D. J. Lichtenwalner, P. Mehta, A. Kingon, D. Zhang, and R. M. Kolbas. 1994. “Light Emission from Crystalline Silicon and Amorphous Silicon Oxide (SiO_x) Nanoparticles,” *Journal of Electronic Materials*, vol. 23, no. 1, pp. 57–62.

Namavar, F., H. P. Maruska, and N. M. Kalkhoran. 1992. “Visible Electroluminescence from Porous Silicon np Heterojunction Diodes,” *Applied Physics Letters*, vol. 60, no. 20, May, pp. 2514–2516.

Newman, R., W. C. Dash, R. N. Hall, and W. E. Burch. 1955. “Visible Light from a Si p-n Junction,” *Physical Review*, vol. 98, pp. 1536–1537.

Offord, B. W. 1992. “Fully-Depleted Silicon-on-Sapphire and Its Application to Advanced VLSI Design,” 4th NASA Symposium on VLSI Design, pp. 4.3.1–4.3.7.

Ohno, T., K. Shiraishi, and T. Ogawa. 1992. “Intrinsic Origin of Visible Light Emission from Silicon Quantum Wires: Electronic Structure and Geometrically Restircted Exciton,” *Physical Review Letters*, vol. 69, no. 16, October, pp. 2400–2403.

Perez, J. M., J. Villalobos, P. McNeill, J. Prasad, R. Cheek, J. Kelber, J. P. Estrera, P. D. Stevens, and R. Glosser. 1992. “Direct Evidence for the Amorphous Silicon Phase in Visible Photoluminescent Porous Silicon,” *Applied Physics Letters*, vol. 61, no. 5, August, pp. 563–565.

Rose, D. J. 1957. “Microplasmas in Silicon,” *Physical Review*, vol. 105, no. 2, pp. 413–418.

Russell, S. D., W. B. Dubbelday, P. Georgief, R. L. Shimabukuro, and P. R. de la Houssaye. 1994a. “The Effects of Microcrystalline Structure on the Photoluminescence of Porous Silicon on Sapphire,” *Journal of Applied Physics*, vol. 76, no. 10, November, pp. 6012–6013.

Russell, S. D., W. B. Dubbelday, P. Georgief, R. L. Shimabukuro, and P. R. de la Houssaye. 1994b. “Porous SOS, BESOS, and SOQ for Flat Panel Emissive Displays,” *1994 IEEE SOI International Conference Proceedings*, pp. 105–106.

Russell, S. D., W. B. Dubbelday, and R. L. Shimabukuro. 1993. “Porous Silicon for Pumping Solid-State Lasers,” NRaD TD 2461 (March). Naval Command, Control and Ocean Surveillance Center, RDT&E Division, San Diego, CA.

Sarathy, J., S. Shih, K. Jung, C. Tsai, K. H. Li, D. L. Kwong, J. C. Campbell, S. L. Yau, and A. J. Bard. 1992. “Demonstration of Photoluminescence in Nonanodized Silicon,” *Applied Physics Letters*, vol. 60, no. 13, pp. 1532–1534.

Sawada, S., N. Hamada, and N. Ookubo. 1994. “Mechanisms of Visible Photoluminescence in Porous Silicon,” *Physical Review B*, vol. 49, no. 8, pp. 5236–5245.

Steiner, P., F. Kozlowski, and W. Lang. 1993. “Blue and Green Electroluminescence from a Porous Silicon Device,” *IEEE Electron Device Letters*, vol. 14, no. 7, July, pp. 317–319.

Wolff, P. A. 1954. “Theory of Electron Multiplication in Silicon and Germanium,” *Physical Review*, vol. 95, September, pp. 1415–1420.

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